

# Digital Pre-Correction Method for Mismatch in DACs with Built-in Self-Measurement

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*Abstract*— In this paper, a solution is proposed for the design of reliable, high-performance current-steering (CS) DACs in modern sub-micron technologies. In addition to the technology-trend of decreasing dimensions, an integration trend of mixed-signal cores with digital systems on a single chip can be observed. While the digital parts benefit from new technologies, the design of accurate, reliable and technology-portable analog circuits becomes more and more complicated. Moreover, the analog cores will be responsible for most of the yield and test problems of the mixed-signal systems-on-chip. The proposed solution is to use a smart approach [1], taking full advantage of on-chip available digital processing power, in order to solve the aforementioned problems.

## I. INTRODUCTION

The current-steering (CS) architecture for digital-to-analog converters (DAC) is the prevailing architecture used for high-speed operation ( $0.1 \sim 1$  GSPS) in combination with moderate resolution ( $10 \sim 16$  bits). Careful design moved the range of operation to higher frequencies [2], and the use of calibration techniques increased the achievable resolution [3], [4]. Nevertheless, the conventional design approach of CS DACs does not take full advantage of the benefits offered by the developments in technology and design. These developments include the shrinkage of IC technologies, the increase of available digital processing power per chip area and the integration of mixed-signal cores in digital systems, leading to mixed-signal systems-on-chip (MSSoC). In spite of these trends, the design of reliable and accurate analog circuitry becomes more complex as newer technologies are less well-defined, stochastic parameters tend to have increased spread, and less voltage headroom is available. In previous work [5], [6], a solution has been proposed using a smart approach: the digital processing power available on-chip in MSSoCs is used to improve performance, reliability, yield and technology-portability, to reduce chip area and to provide on-chip correction and

test functionality. In this paper, transistor-level simulations verify the validity of the previously proposed solution.

In section II, the conventional approach to design DACs is discussed. Then, the new approach is presented in section III and simulation results are given in section IV. Finally, conclusions are drawn in section V.

## II. CONVENTIONAL DESIGN APPROACH

In this section, the conventional approach to design a DAC for a specific accuracy is discussed briefly. For simplicity of explanation, a fully binary-weighted architecture is considered here. An  $N$ -bit binary converter is conventionally composed of  $2^N - 1$  unit current cells (each with current  $I_u$  ideally), grouped in  $N$  branches using a binary scale: branch  $i$  ( $0 \leq i < N$ ) contains  $2^i$  unit cells. Due to technology imperfections, the currents produced by each unit cell are subject to a stochastic deviation with relative spread  $\frac{\sigma_u}{I_u}$ . This spread is a function of the dimensions of the transistor operating as a current source, according to [7]:

$$\frac{\sigma_u}{I_u} \propto \frac{1}{\sqrt{WL}}, \quad (1)$$

where  $W$  is the width and  $L$  the length of the unit transistor. In order to achieve a certain accuracy of the converter, a minimum size of the transistors in the unit cells is required. According to [8], for an  $N$ -bit converter with a maximum INL error of 0.5 LSB with a  $3\sigma$  confidence level, the maximum tolerated relative spread can be estimated by:

$$\frac{\sigma_u}{I_u} = \frac{1}{6\sqrt{2^{N-1}}} \quad (2)$$

Especially for higher resolutions ( $\geq 12$  bits), this constraint leads to a large chip area. Although calibration techniques are able to relax the constraint somewhat [3], [4], they require an additional CALDAC to compensate for the deviations of the current cells, and

moreover, the improvement in accuracy is limited to a few bits. To overcome these limitations, an alternative design approach was presented in [5], [6], based on a DAC with redundancy, digital pre-correction and built-in self-measurement. With this approach, the achievable accuracy of the converter ( $N$ -bit) is decoupled from the intrinsic accuracy of the current sources  $\frac{\sigma_u}{I_u}$ . Therefore, the new approach can achieve minimum area independent of the target accuracy, no additional accurate analog components (like the CAL-DAC) have to be designed, and the technique is less sensitive to other design issues like spatial parameter deviations, systematic layout deviations and deviations in technology parameters.

### III. DIGITALLY PRE-CORRECTED DAC WITH REDUNDANCY

In this section, the design approach as presented in [5], [6] is rehearsed. The most important goal of this approach is to take full advantage of the technology and design trends by minimizing the chip area (made possible by the technology trend) and to use digital pre-correction (made affordable by the MSSoC trend) to solve the problems related to small chip area. On top of that, it will be shown that the approach is suitable to enhance reliability, technology-independence and yield as well.

#### A. System Overview

A general view of a digitally pre-corrected DAC is given in fig. 1. In order to take maximum advantage of technology-scaling, the physical size of the current sources is not chosen according to equations (1) and (2), but minimized as much as possible instead. The resulting large mismatch of the current sources is not corrected by analog means (e.g. CALDACs), but by re-mapping the binary input codes to appropriate combinations of current sources. A built-in measurement algorithm is used to measure the actual deviations of the individual current sources, such that the digital pre-correction algorithm can determine a suitable combination of current sources for each input code.

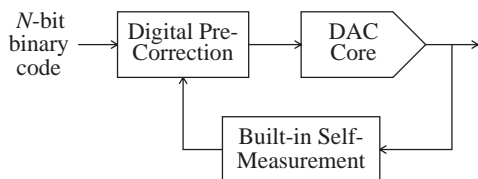


Fig. 1. Digitally pre-corrected DAC with built-in self-measurement.

With pre-correction, not all types of mismatch errors can be corrected. Fig. 2 shows the two possible types of error due to mismatch of the MSB of a binary DAC; a comparable situation can occur with the other sources of the DAC. The large DNL error produced in the left picture can not be reduced with pre-correction, as there is no combination of current sources available to fill the gap in the output range. On the other hand, the error in the right picture can be corrected with pre-correction, by simply omitting a few codes. However, the full-scale range of this converter will be slightly smaller than usual. When the

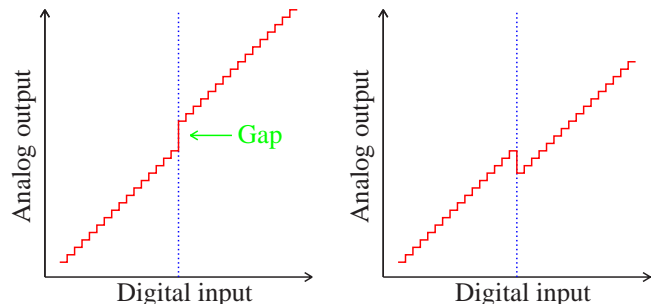


Fig. 2. Possible effects of mismatch of the MSB: a ‘positive’ (left) and a ‘negative’ (right) deviation of the MSB.

situation of fig. 2 (left) can be avoided under all circumstances, the pre-correction is able to correct all deviations due to mismatch of the current sources. This requirement can be guaranteed with arbitrary high certainty by the use of redundancy.

The three components of the system (redundancy, built-in self-measurement and digital pre-correction) will be discussed separately in the following sections. It should also be noticed that previous work on digitally pre-corrected DACs exists [9], but this work does not show mathematical analysis, uses a sub-optimal redundancy distribution and uses a more complex measurement method.

#### B. Redundancy

A normal  $N$ -bit binary converter is composed of  $k = N$  current sources. These sources  $I_0$  (LSB) up to  $I_{k-1}$  (MSB) are chosen relatively to the unit element  $I_u$  using the ratios  $\alpha_0$  up to  $\alpha_{k-1}$ . The ratios  $\alpha_i$  are chosen such that each source is exactly 1 LSB larger than the sum of all smaller sources:

$$\alpha_j = \sum_{i=0}^{j-1} \alpha_i + 1 \text{ for } 0 \leq j < k, \quad (3)$$

leading to the sequence of  $\alpha$ ’s: 1, 2, 4, 8, 16, ... However, when due to mismatch one of the current

sources is actually larger than expected, a 'gap' (as in fig. 2) arises, that can not be corrected with digital pre-correction. To avoid this situation, redundancy is added such that  $\alpha_j$  is intentionally smaller than the sum of all smaller sources plus one LSB:

$$\alpha_j < \sum_{i=0}^{j-1} \alpha_i + 1 \text{ for } 0 \leq j < k \quad (4)$$

An example of a sequence, fulfilling this constraint, is e.g.: 0.7, 1.3, 2.4, 4.6, 8.8, ... The more redundancy is added, the more severe deviations due to mismatch can be compensated by pre-correction. However, also note that the more redundancy, the more sources  $k$  have to be employed as the redundancy reduces the full-scale range of the converter.

Due to the stochastic spread of the unit cells, the actual value of each source becomes a stochastic value  $\underline{\alpha}_i$  with mean  $\alpha_i$  (the designed value) and spread  $\sqrt{\alpha_i \frac{\sigma_u}{I_u}}$ . To guarantee that all required output levels can be produced with sufficient accuracy using pre-correction, the relations from (4), taking the stochastic spread of the sources into account, have to be fulfilled. This leads to the following set of requirements:

$$\underline{C}_j > 0 \text{ for } 0 \leq j < k, \text{ with:} \quad (5)$$

$$\mathbf{E}\{\underline{C}_j\} = 1 - \alpha_j + \sum_{i=0}^{j-1} \alpha_i$$

$$\sigma_{\underline{C}_j} = \frac{\sigma_u}{I_u} \sqrt{\sum_{i=0}^j \alpha_i},$$

where  $\mathbf{E}\{\underline{C}_j\}$  is the expectation of  $\underline{C}_j$  and  $\sigma_{\underline{C}_j}$  is the spread of  $\underline{C}_j$ . When all constraints  $\underline{C}_j$  are fulfilled, the target accuracy can be achieved by the use of pre-correction. The desired probability of fulfilling each constraint  $\underline{C}_j$  can be expressed as a desired level of confidence  $\lambda\sigma$  with which the constraint has to be fulfilled:

$$P\{\underline{C}_j > 0\} = 1 - \frac{1}{2} \operatorname{erfc}\left(\frac{\lambda}{\sqrt{2}}\right) \quad (6)$$

The confidence level requires that:

$$\mathbf{E}\{\underline{C}_j\} - \lambda\sigma_{\underline{C}_j} = 0 \quad (7)$$

Using equations (5) and (7), the values of  $\alpha_j$  can be derived given the relative spread of the unit cells and a desired confidence level:

$$\alpha_j = \frac{x_j - \sqrt{x_j^2 - 4y_j}}{2}, \text{ with:} \quad (8)$$

$$x_j = 2 \left( 1 + \sum_{i=0}^{j-1} \alpha_i \right) + \lambda^2 \left( \frac{\sigma_u}{I_u} \right)^2 \quad \text{and}$$

$$y_j = \left( 1 + \sum_{i=0}^{j-1} \alpha_i \right)^2 - \lambda^2 \left( \frac{\sigma_u}{I_u} \right)^2 \sum_{i=0}^{j-1} \alpha_i$$

As opposed to [9], who used a fixed sub-binary radix (i.e. a fixed ratio  $\alpha_{j+1}/\alpha_j$  less than 2), the presented approach for designing the current sources results in a variable radix. By adapting the radix, the error probability for each source is equalized, whereas a fixed radix results in a variable error probability. As a result, the presented approach achieves the same yield with less redundancy and hence less current sources and less chip area.

### C. Built-in Self-Measurement

Before being able to pre-correct the mismatch errors of the current sources, a measurement procedure, measuring the actual values of the current sources, is required. After performing the self-measurement procedure at power-up, the actual values of the current sources are known in the digital domain, and the converter can start its normal operation.

In order to implement the measurement technique on-chip, it has to fulfill several constraints: it has to be reliable, accurate, small, and realizable on-chip. Moreover, it is undesirable to modify the DAC-core to support the measurement procedure by means of additional switches or sources, as this could influence (dynamic) performance of the DAC adversely. To comply with all these constraints, the setup of fig. 3 is proposed. It uses a simple analog measurement circuit (composed of a band-pass filter (BPF) and a comparator), and a digital measurement algorithm, controlling the current sources in the DAC-core during the self-measurement.

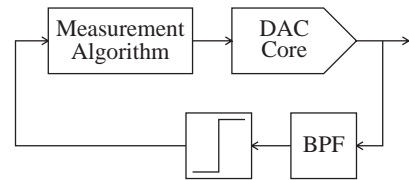


Fig. 3. Detailed view of the built-in self-measurement setup, composed of a band-pass filter, a comparator and an algorithm.

#### C.1 Measurement Algorithm

The measurement algorithm, comparable to the approach in [9], is aimed at minimizing analog circuitry

of the measurement technique by using digital algorithms as much as possible. Instead of measuring the values of the current sources in an absolute sense (which would require an accurate ADC), sources are measured relatively to each other only.

The idea of the method is to find for each current source  $j$  a combination of current sources 0 up to  $j-1$ , of which the combined output current  $I_{sum,j}$  approximates the actual current  $I_j$  of source  $j$  as good as possible. As the measurement is a *relative* measurement, the actual values of  $I_j$  and  $I_{sum,j}$  are not important, it is sufficient to determine the combination of sources which minimizes  $|\Delta_j| = |I_j - I_{sum,j}|$ .  $I_{sum,j}$  can be written as:

$$I_{sum,j} = \sum_{i=0}^{j-1} S_{i,j} \cdot I_i, \quad (9)$$

where  $I_i$  is the actual current of source  $i$ , and  $S_{i,j} = 0$  when source  $i$  is not used and  $S_{i,j} = 1$  when source  $i$  is used in the combination approximating  $I_j$ . The combination of sources composing  $I_{sum,j}$  can be found using a comparator determining the sign of  $\Delta_j$ , and a successive-approximation algorithm minimizing  $|\Delta_j|$  by controlling the current sources. In the actual design, a BPF was added to the analog circuit, but this will be explained in section III-C.2. The measurement algorithm determines the values of  $S_{i,j}$ , based on which the digital representation  $\omega_j$  of each current source  $j$  can be derived:

$$\omega_j = \sum_{i=0}^{j-1} S_{i,j} \cdot \omega_i \quad (10)$$

The measurement algorithm starts with initializing the digital representation of the smallest source (source 0)  $\omega_0$  to 1, an arbitrary unit value. Then, iteratively for all other sources  $j$ , starting with source 1, up to source  $k-1$ , the measurement procedure determining  $I_{sum,j}$  is performed, and the digitized estimation  $\omega_j$  can be derived. The algorithm determining  $\omega_j$  is illustrated in fig. 4. This algorithm is performed iteratively for the sources 1 up to  $k-1$ .

### C.2 Analog Measurement Circuit

The analog part of the measurement setup has to provide the digital algorithm with the sign information of  $\Delta_j$ . In [9], a two-step approach is used. First the value of  $I_j$  is recorded on a variable current source (implemented as a sub-binary DAC). In the second step, the recorded value is compared to  $I_{sum}$ , yielding the sign of  $\Delta_j$ . The main disadvantage of this method is that it requires a complete

```

Turn off all sources ( $I_{sum} = 0$ )
for  $i = j - 1$  down to 0
    Turn on source  $i$  ( $I_{sum} = I_{sum} + I_i$ )
    if  $I_{sum} > I_j$ 
         $S_i = 0$ 
        Turn off source  $i$  ( $I_{sum} = I_{sum} - I_i$ )
    else
         $S_i = 1$ 
    end if
end for

```

Fig. 4. Algorithm, finding a combination of sources approximating source  $j$ .

DAC, of which the accuracy limits the accuracy of the measurement. Moreover, due to this implementation, the unit elements in the DAC-core have to be disconnected from the normal output and reconnected to the measurement circuitry by means of a switch. When this implementation is to be used for high-performance current-steering DACs, this additional switch consumes voltage-headroom (which can be critical in modern low-voltage technologies) and possibly degrades dynamic performance as well. Therefore, another approach is proposed here requiring neither an additional DAC in the measurement setup nor a switch at the output of the DAC-core as it can be connected to the DAC's output permanently.

It is assumed that the current-steering DAC is designed as a differential DAC, which is the case for almost any high-performance DAC nowadays. In this situation, the DAC has a positive and a negative output, and the current of each source  $j$  is connected to either of the two outputs. During the measurement of source  $j$ , it is not possible to disconnect the sources not taking part in the algorithm (i.e. all sources  $i$  with either  $S_{i,j} = 0$  or  $i > j$ ). In order to distinguish the information to be measured from the superfluous information, the information to be measured is modulated on a carrier signal: The DAC continuously alternates between two states  $\phi_1$  and  $\phi_2$ . All sources not taking part in the measurement remain connected to the negative output of the DAC, resulting in a DC output current  $I_{DC}$ . Source  $j$  (the source of which the value has to be determined) is connected to the positive output during phase  $\phi_1$  and to the negative output during phase  $\phi_2$ . All sources  $i$  with  $S_{i,j} = 1$  are connected to the negative output during phase  $\phi_1$  and to the positive output during phase  $\phi_2$ . Fig. 5 illustrates the output of the DAC as a function of time.

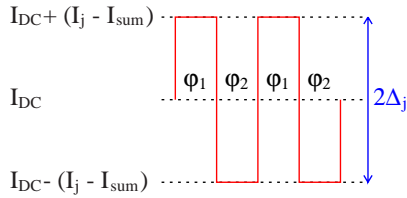


Fig. 5. DAC output as a function of time during the self-measurement of source  $j$ .

When a band-pass filter is connected to the output of the DAC, the DC level is blocked, and hence the comparator is provided only by the information to be measured. The output of the comparator becomes a square wave, of which the phase (with respect to  $\phi_1$  and  $\phi_2$ ) corresponds to the sign of  $\Delta_j$ , the information required by the digital measurement algorithm.

#### D. Digital Pre-Correction Algorithm

The digital pre-correction algorithm has to select a suitable combination of current sources for each possible input code, based on the measurement results of the actual values of the sources (the values  $\omega_j$ ). A successive-approximation algorithm (fig. 6) is used to find a suitable combination: starting with the largest source  $j = k - 1$ , the values  $\omega_j$  are either added to or subtracted from the input code, such that the residual value is minimized. Corresponding to this addition or subtraction, the actual source is connected to the negative or the positive output of the DAC respectively.

$residue \leftarrow$ ‘new input code’
for $i = k - 1$ down to 0
if $residue \geq 0$
select $w_i$ positive
$residue = residue - w_i$
else
select $w_i$ negative
$residue = residue + w_i$
end if
end for

Fig. 6. Digital pre-correction algorithm.

## IV. SIMULATION RESULTS

In this section, simulation results for a digitally pre-corrected DAC are presented. For comparison, results are also given for a conventionally designed converter.

#### A. Conventional Converter

A design example for a 12-bit converter is considered in this section. In case of a conventional design,

12 current sources are used to construct the converter. According to (2),  $\frac{\sigma_u}{I_u} = 0.37\%$  is required for 12-bits accuracy.

Monte-Carlo simulations were performed on 1 million converters using a high-level DAC model in C-language. Each unit-source was given a random mismatch using a Gaussian distribution with mean 0 and  $\frac{\sigma_u}{I_u} = 0.37\%$ . The maximum INL error and maximum DNL error were determined for each converter. 99.9879% of all converters achieved a maximum INL less than 0.5 LSB, and 96.2706% of all converters achieved a maximum DNL less than 0.5 LSB.

#### B. Digitally Pre-Corrected Converter

As in the previous section, the design of a 12-bit converter is considered here. As opposed to the conventional design, where  $\frac{\sigma_u}{I_u}$  is determined by the target accuracy, in this situation,  $\frac{\sigma_u}{I_u}$  can be chosen independent of the target accuracy.  $\frac{\sigma_u}{I_u}$  was set to 7.5% as this enables a significant reduction of active area compared to the conventional design (up to a factor 400 gain in area, according to (1)), but also provides an ‘error budget’ to cover deviations for several ill-defined processes that are hardly quantifiable (like systematic layout deviations, deviations of technology parameters, etc.). Based on (8), the ideal values of the current sources can be calculated, resulting in the values given in table I. As explained before, due to the redundancy, more than 12 current sources will be required to achieve 12-bit final accuracy. Simulations will show that 16 sources are sufficient. With less than 16 sources, 12-bit accuracy is not achieved and with more than 16 sources, the final accuracy will become better than required.

Current Source	Designed Value	Current Source	Designed Value
$\alpha_0$	0.7416	$\alpha_8$	130.1583
$\alpha_1$	1.3118	$\alpha_9$	258.3352
$\alpha_2$	2.4190	$\alpha_{10}$	513.8702
$\alpha_3$	4.5702	$\alpha_{11}$	1023.7815
$\alpha_4$	8.7762	$\alpha_{12}$	2041.9654
$\alpha_5$	17.0474	$\alpha_{13}$	4076.0152
$\alpha_6$	33.3877	$\alpha_{14}$	8140.8366
$\alpha_7$	65.7807	$\alpha_{15}$	16265.8430

TABLE I

VALUES OF THE CURRENT SOURCES DESIGNED FOR 12-BIT FINAL ACCURACY, ASSUMING  $\frac{\sigma_u}{I_u} = 7.5\%$  UNIT-CELL MISMATCH AND  $4\sigma$  CONFIDENCE LEVEL.

As in section IV-A, 1 million converters were used in a Monte-Carlo simulation, where each unit-source was given a mismatch corresponding to  $\frac{\sigma_u}{I_u} = 7.5\%$ . An implemented measurement algorithm was used to determine the digital coefficients representing the values of the current sources (according to section III-C), based on which the digital pre-correction algorithm (according to section III-D) was initiated. Fig. 7 shows the achieved INL and DNL for these converters. Despite the large mismatch of 7.5%, 99.9986% of all converters achieved their INL specification, and 99.9967% of all converters achieved their DNL specification. Especially the DNL has improved over the conventional design, which is due to the binary-weighted architecture which inherently results in large DNL errors. Conventionally, these DNL errors are circumvented by using a segmented architecture. However, the large DNL errors normally associated with binary-weighted architectures are removed automatically when redundancy with pre-correction is employed, as the measurement algorithm basically minimizes the DNL error by minimizing  $\Delta_j$  (section III-C).

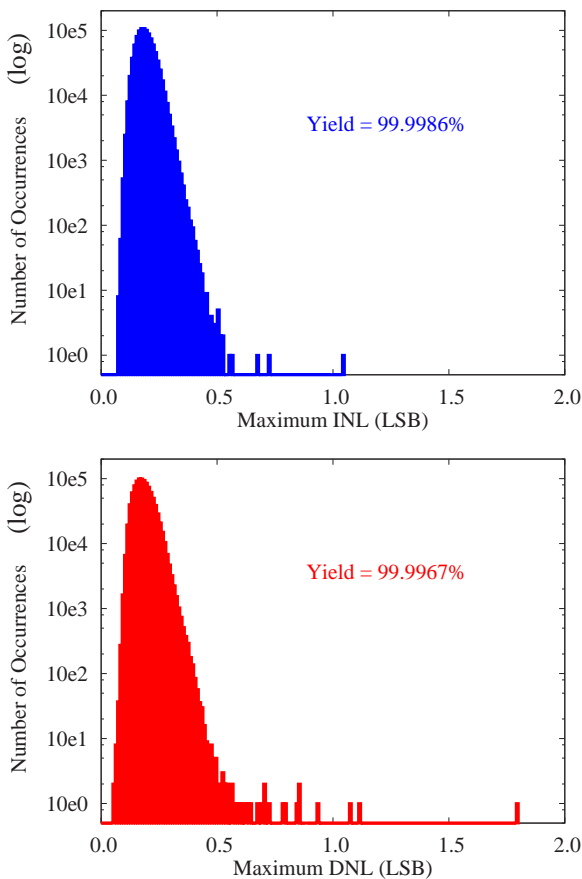


Fig. 7. Maximum INL (top) and maximum DNL (bottom) for 1 million digitally pre-corrected converters.

### C. Transistor-Level Simulations

To verify the performance of a digitally pre-corrected DAC using transistor-level simulations, two 12-bit DACs (according to the examples from IV-A and IV-B) were designed on transistor-level. A standard  $0.18\mu\text{m}$  CMOS technology (UMC18) was selected to implement the designs. Both DACs (the conventional DAC and the digitally pre-corrected DAC) share exactly the same building blocks (latches, switch-drivers, switches, etc.), except for the physical sizes of the current source transistors. The schematic of the unit current cell is given in fig. 8. The switches ( $M_3$  and  $M_3'$ ) are driven by the digital input code ( $D$  and  $/D$ ) using a switch-driver. The cascode transistors ( $M_2$ ,  $M_4$  and  $M_4'$ ) are used to increase the output impedance of the unit cell. The size of the current source transistor  $M_1$  is chosen dependent on the tolerated mismatch. The conventional DAC design requires unit current cells with  $\frac{\sigma_u}{I_u} = 0.37\%$ , resulting in transistors with an area of more than  $200\mu\text{m}^2$  ( $\frac{W}{L} = \frac{16\mu\text{m}}{14\mu\text{m}}$ ). On the other hand, for the unit cells of the digitally pre-corrected DAC, a mismatch of  $\frac{\sigma_u}{I_u} = 7.5\%$  can be tolerated, resulting in transistors with an area of only  $0.24\mu\text{m}^2$  ( $\frac{W}{L} = \frac{0.45\mu\text{m}}{0.55\mu\text{m}}$ ).

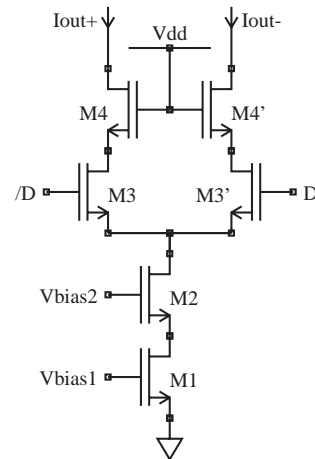


Fig. 8. Unit current cell, composed of current source ( $M_1$ ), switches ( $M_3$  and  $M_3'$ ) and cascodes ( $M_2$ ,  $M_4$  and  $M_4'$ ).

To verify the performance of the pre-corrected DAC, mismatch with a relative spread of  $\frac{\sigma_u}{I_u} = 7.5\%$  was added on purpose to all current sources. As the measurement circuit was not yet implemented, the measurement procedure according to section III-C was carried out in Matlab. The results were used to pre-correct the transistor-level DAC using a VHDL-code implementation of the algorithm from section III-D. Fig. 9 shows typical INL and DNL curves that were obtained from these simulations.

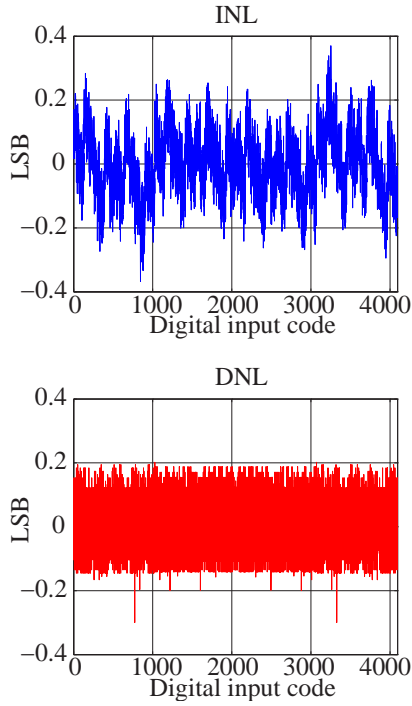


Fig. 9. Typical INL (top) and DNL (bottom) for a digitally pre-corrected DAC with 7.5% unit source mismatch.

In order to compare the dynamic performance of the digitally pre-corrected DAC with the conventional DAC, three different configurations were simulated:

- A) conventional DAC, with ideally matched current sources;
- B) digitally pre-corrected DAC, with ideally matched current sources;
- C) digitally pre-corrected DAC, using unit current cells taking mismatch with a relative spread of  $\frac{\sigma_u}{I_u} = 7.5\%$  into account.

Configurations **A** and **B** consider a nominal situation, while configuration **C** considers a worst-case situation.

The three configurations were provided with an input sine of 29MHz while a sample frequency of 500MSPS was used. Figures 10, 11 and 12 show the output spectra of configuration **A**, **B** and **C** respectively.

In the figures, it can be seen that the SNDR is equally good for all three configurations (69.1dB up to 70.9dB). However, with respect to SFDR, the digitally pre-corrected DAC achieves around 5dB better performance than the conventional DAC. This improvement even holds when the pre-corrected DAC experiences 7.5% mismatch in the unit current cells. The performance improvement of the pre-corrected DAC probably stems from the reduced parasitic capacitances of the unit current source transistors.

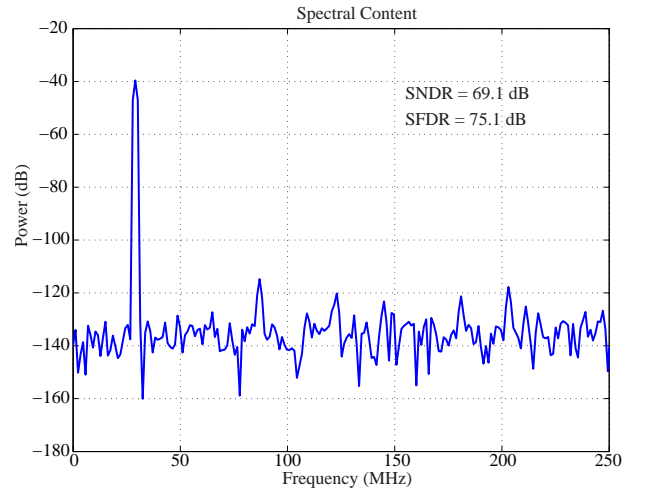


Fig. 10. Single tone output spectrum of a conventional DAC without mismatch of the current sources.

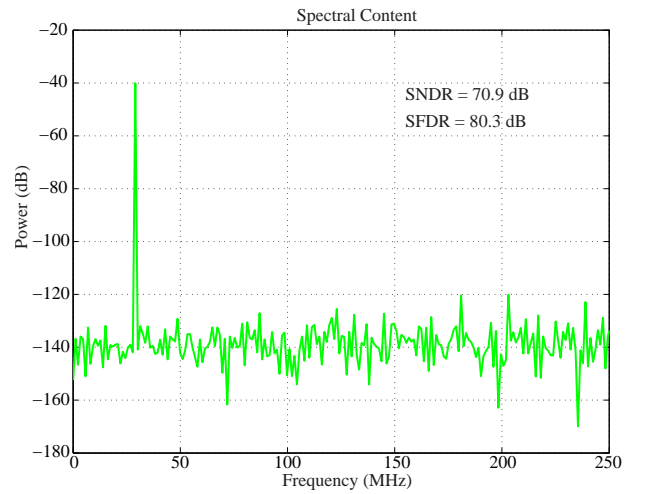


Fig. 11. Single tone output spectrum of a digitally pre-corrected DAC without mismatch of the current sources.

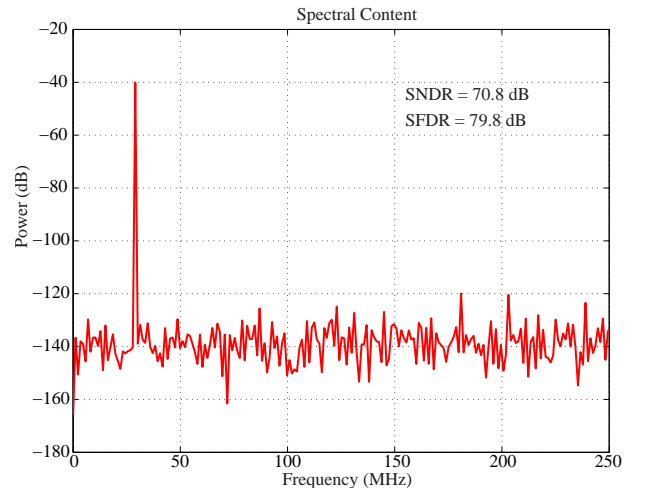


Fig. 12. Single tone output spectrum of a digitally pre-corrected DAC with 7.5% unit source mismatch.

## V. CONCLUSION

In this paper, it was shown that with redundancy, digital pre-correction and built-in self-measurement, high-accuracy DACs can be designed virtually independent of device mismatch, significantly reducing chip area and making the design less dependent on exact technology parameters. The novel approach is especially useful for high-accuracy DACs where the overall chip area is dominated by the area occupied by the current-source transistors.

A novel optimized-redundancy approach using a variable sub-binary radix was introduced, which optimizes the distribution of the redundancy amongst the individual sources and therefore maximizes overall yield. Also, a novel self-measurement method was introduced, removing the necessity of a temporary DAC inside the measurement setup and circumventing any modification of the DAC-core.

Transistor-level simulations showed that a digitally pre-corrected DAC with an intrinsic mismatch of 7.5% outperforms a conventionally designed converter with 0.37% mismatch with respect to both static and dynamic performance.

It can be concluded that the presented approach achieves high reliability, high accuracy, small chip area and embedded test functionality at the same time, resulting in reduced production costs, reduced test costs and higher yield.

## VI. ACKNOWLEDGEMENTS

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