Analog Calibration of an Open-Loop Track-and-Hold Circuit

Pieter Harpe, Athon Zanikopoulos, Hans Hegt, Arthur van Roermund
Mixed-signal Microelectronics Group, Eindhoven University of Technology,
PT 5.13, P.O.Box 513, 5600 MB Eindhoven, The Netherlands
email: p.j.a.harpe@tue.nl, phone: +31 40 247 4703, fax: +31 40 245 5674

Abstract— **This paper presents a method for the on-chip measurement and correction of gain errors, offsets and non-linearities of a Track-and-Hold circuit (T&H) of an ADC. Open-loop T&H circuits will be considered in this paper because of their high-speed and low-power capabilities. However, these open-loop circuits require calibration for the aforementioned errors in order to achieve a high accuracy, especially in case of time-interleaved architectures. With the proposed method, the errors can be measured and digitized on-chip accurately, without requiring a substantial amount of hardware or any accurate references. Then, this information is used by a digitally implemented algorithm to optimize several controllable analog parameters of the circuit. In turn, these parameters minimize the effect of mismatch errors. After optimization, the digital logic can be switched off completely in order to save power.**

I. Introduction

Observing trends in recent designs of analog-to-digital converters (ADCs), several key elements that enable high-speed and high-accuracy can be identified. These elements are parallelism, open-loop circuitry and calibration or correction methods. Parallelism is achieved by time-interleaving multiple ADCs to achieve a higher overall sampling frequency [1]. Open-loop circuits in general are able to achieve high-speed and low power-consumption because of the absence of feedback and the use of smaller components, reducing parasitics [2]. Finally, calibration or correction techniques can be used to enhance the accuracy of the system, which becomes especially useful in case of open-loop structures [3]. Targeting an ADC including all the previously mentioned key elements, we focus here on the correction technique of a front-end T&H circuit, as the T&H is an important bottleneck in the design of high-speed ADCs. For reasons of power efficiency, an analog correction method was developed [4], as opposed to the majority of techniques, which is implemented in the digital domain (e.g. [3], [5]). Our design goal is to achieve a 10-bit accurate 500MSPS T&H, which has to be suitable for a time-interleaved architecture.

In section II, an open-loop T&H circuit is presented, and its use in a time-interleaved architecture will be discussed. Section III presents the self-measurement and self-correction technique for the optimization of the accuracy, and simulation results on behavioral and transistor-level are presented in sections IV and V, followed by conclusions in section VI.

II. Open-Loop Circuits in Time-Interleaved ADCs

A. Proposed Open-Loop T&H Circuit

The proposed open-loop T&H circuit (fig. 1) designed in a 0.18μm CMOS technology was presented previously in [6]. Therefore, it will be discussed just briefly here. The applied differential input voltage (max. ±0.5V) is sampled on the two sampling capacitors (C_s) using simple NMOS switches, driven by a boosted clock signal [7]. An open-loop buffer is used to drive the ADC. The linearity of the buffer is improved by using both cross-coupling and source degeneration [8]. Simulation results (fig. 2 and 3) show that this circuit achieves 62dB SFDR while operating at 500MSPS and consuming 15mW power.

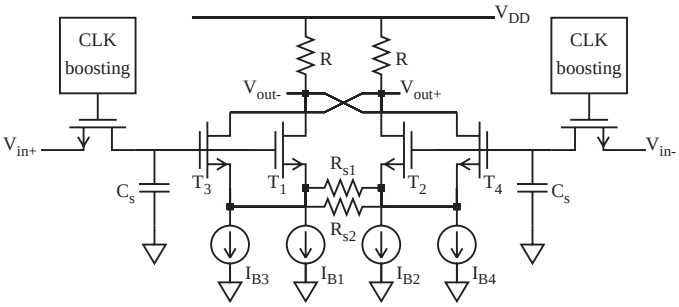

Fig. 1. Open-loop Track-and-Hold circuit, based on a cross-coupled differential pair with source degeneration.

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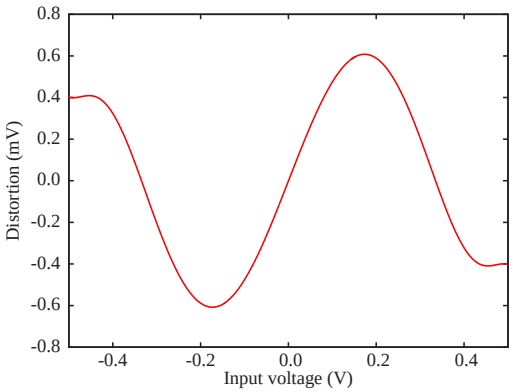

Fig. 2. Simulated static performance of the T&H circuit.

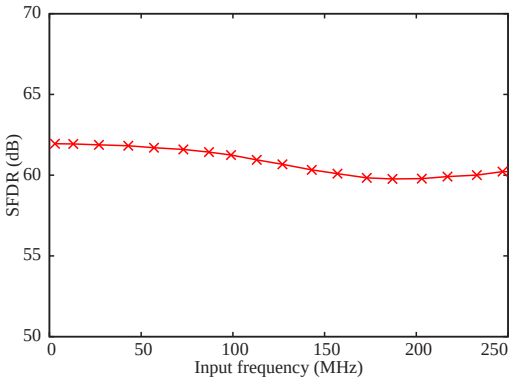

Fig. 3. Simulated dynamic performance of the T&H.

B. Application in Time-Interleaved Architectures

When the proposed T&H circuit is to be used in time-interleaved ADCs, the requirements on matching of gain and offset between the channels become crucial [9]. As an estimation, we use here the constraint that the offset and gain error should be $0.5LSB$ of the ADC resolution N at most. Assuming an analog input-range of $\pm V_{fs}$, this value equals $0.5LSB = \frac{V_{fs}}{2^N}$, yielding the following set of constraints for the offset o_e and gain error g_e for an N bits ADC:

$$|o_e| \leq \frac{V_{fs}}{2^N} \quad \text{and} \quad |g_e| \leq \frac{1}{2^N} \tag{1}$$

The presented T&H circuit is intrinsically (due to mismatch) not accurate enough to fulfill these constraints for an $N = 10$-bit time-interleaved ADC. Therefore, a mismatch correction method is necessary for such an application.

C. Analog Parameters for Mismatch Correction

In reality, all components used in fig. 1 will suffer from mismatch. As the circuit was designed for high-speed, these components are small in physical size, resulting in a relatively large amount of mismatch. Moreover, in an open-loop circuit, there is no feedback to reduce the mismatch effects. In this paper, we focus on the mismatch errors of the open-loop buffer, as it is the dominant source of errors. The transfer function of this buffer can be expressed as:

$$V_{out} = o_e + (1 + g_e)V_{in} + HD_{even}(V_{in}) + HD_{odd}(V_{in}) \tag{2}$$

In this expression, o_e is the offset, g_e the gain-error, HD_{even} the even-order distortion and HD_{odd} the odd-order distortion due to both mismatch and limited intrinsic linearity of the buffer. The goal of our correction technique is to minimize these four effects by analog means. The main advantage of analog correction is that it does not increase power consumption as opposed to digital correction. To implement the analog correction means, the four current sources I_{B1} up to I_{B4} (see fig. 1) are made digitally programmable. These four variable sources provide enough degrees of freedom to minimize the mismatch effects of all components at the same time to the desired level. In principle, a trade-off exists between the required intrinsic performance of the circuit, and the required additional performance of the calibration technique: a more simple circuit will need a more complex calibration circuit and vice versa. However, this trade-off exists mainly with respect to the overall chip-area. Here, the design is optimized with respect to speed. As the calibration circuit is implemented by means of the programmability of the *static* current sources of the differential pairs, it has little impact on the speed. Therefore, the optimal solution is to shrink the circuit as much as possible (achieving the highest possible speed), and rely as much as possible on calibration. Based on this observation, each variable current source is implemented with 9 NMOS devices in parallel: 1 large device which is always turned on, providing a nominal current I_{nom}, and 8 binary-scaled transistors of smaller dimensions, that can be turned on or off individually by digital control signals. In this way, each source can be set individually to one out of 256 values:

$$I_{B_x} = I_{nom_x} \cdot (1 + 0.25 \cdot p_x/255) \ , \tag{3}$$

where p_x is the digital control signal for source x, varying from 0 to 255. The span of the programmable part of the source (in this case $0.25 \cdot I_{nom}$) was chosen such that it can cover the most extreme cases of mismatch, while the smallest possible current step (in this case $0.25 \cdot I_{nom}/255$) is small enough to ensure that the correction can be made accurate enough. Together, this results in an 8-bit programmable source. Fig. 4 shows

the implementation of a variable current source; for simplicity only three out of the eight programmable elements are shown.

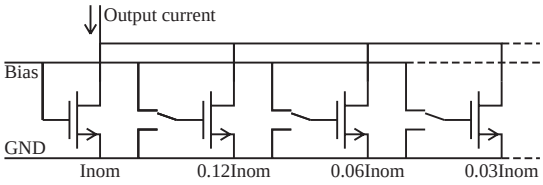

Fig. 4. Implementation of the controllable current sources.

Figures 5 up to 8 show the effect of the programmable current sources on the gain, offset, odd-order distortion and even-order distortion, respectively. In each figure, the nominal situation is plotted and compared against the two corner situations (by tuning the relevant current sources to either the maximum or the minimum value). From this, one can see that with the designed current sources, the gain can be controlled between ±8% of the nominal value and the offset between ±80mV. The linearity compensation plots show that the odd-order and even-order distortions can be controlled within a certain range. Numerical results on the linearity improvement will be shown later.

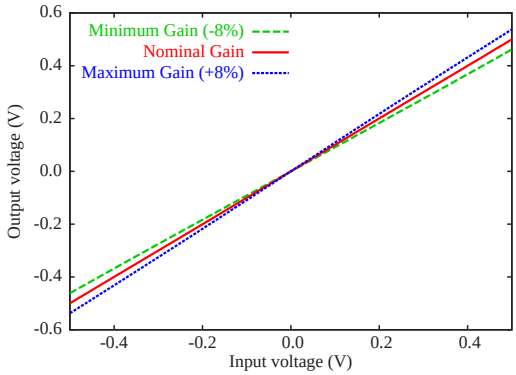

Fig. 5. Gain controllability.

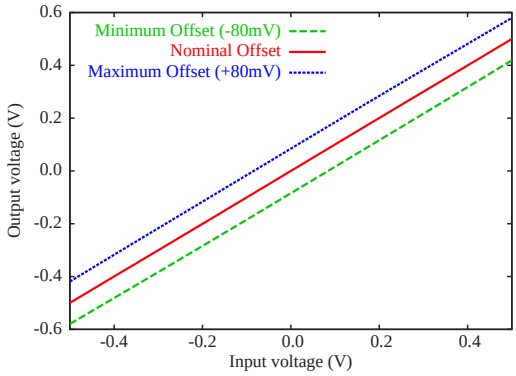

Fig. 6. Offset controllability.

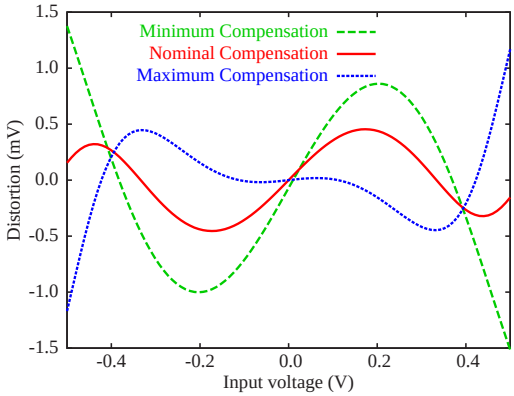

Fig. 7. Odd-order distortion controllability.

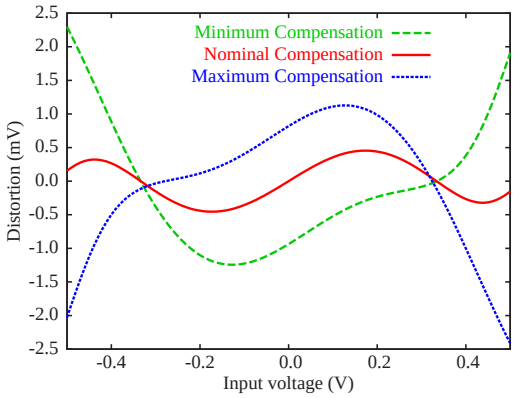

Fig. 8. Even-order distortion controllability.

In the next section, the methods to measure the non-idealities, and to optimize the four controllable parameters p_x based on the measured information will be introduced. These algorithms are implemented in the digital domain, but they are used only during calibration and can be turned off during normal operation of the converter. Therefore, their power consumption is not critical for the overall performance.

For simplicity, a single-channel ADC will be considered in the following. For a time-interleaved ADC, the correction procedure has to be applied to each individual channel separately.

III. Digitally Assisted Analog Correction

A. Self-Measurement Method

For the on-chip measurement of the T&H circuit, the setup previously presented in [10] will be used, see fig. 9. A small 6-bit DAC is used to generate a set of $2^6 = 64$ static test signals. By means of a switch, either the analog input x or the output y of the T&H is selected and digitized by the ADC. In this way, each input code i (with $0 \leq i \leq 63$) of the DAC results in two output codes of the ADC: one with the T&H inserted (yielding code y_i) and one with the T&H by-

passed (yielding code x_i). When the T&H circuit is ideal, these codes must be equal: $x_i = y_i$. Each difference between x_i and y_i indicates a non-ideality of the T&H. Note that these observations remain valid regardless of any static error in the DAC or ADC, like e.g. offset or non-linearity. Therefore, this measurement method is insensitive to the accuracy of the DAC and the ADC, which enables simple on-chip integration. After calibration, the DAC is disconnected and normal operation can start.

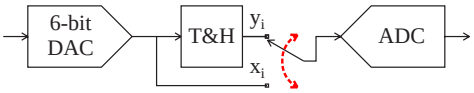

Fig. 9. Self-measurement setup for the T&H circuit.

B. Optimization Algorithm

The goal of the optimization algorithm is to minimize iteratively the differences between x_i and y_i by tuning the four programmable current sources. Instead of using a blind approach, the knowledge of the circuit and its behavior as a function of the parameters is used to reduce the complexity of the algorithm. Each iteration of the algorithm starts with a self-measurement cycle (section III-A). From these results, estimations of the different errors (o_e, g_e, HD_{even} and HD_{odd} as in (2)) are extracted. With these error estimations, the parameters p_x of the current sources are updated. After this update, a new iteration is started until a stable parameter solution is found. In the following, the error estimation will be discussed first, and then the parameter update.

As the measured codes x_i represent the input of the T&H and the codes y_i represent the output, the offset and gain-error can be estimated easily by means of a linear-fit in the least-squares sense using the data points (x_i, y_i). Then, only a residual signal d_i remains, which is the difference between the actual data points and the linear estimation:

$$d_i = y_i - \left(\hat{o_e} + (1 + \hat{g_e})x_i\right) , \tag{4}$$

where $\hat{o_e}$ is the offset estimation and $\hat{g_e}$ the gain-error estimation. The remaining difference d_i corresponds to the non-linearity of the T&H. As the required parameter update is different for even and odd order distortion, two separate quantities $\hat{even}$ and $\hat{odd}$ are used to quantify even and odd order distortion, respectively. For this goal, we exploit the fact that the DAC is differential and produces both positive and negative levels of equal magnitude, such that the sum of these DAC levels equals zero:

$$\sum_{i=0}^{63} x_i = 0 \tag{5}$$

Likewise, all odd harmonic functions of x_i add up to zero because of their symmetry, but on the other hand, all even order harmonic functions of x_i add up to a non-zero value. The estimations $\hat{even}$ and $\hat{odd}$ are defined such that even order distortion contributes only to $\hat{even}$, and odd order distortion only to $\hat{odd}$:

$$\hat{odd} = \sum_{i=0}^{63} d_i x_i^3 \tag{6}$$

$$\hat{even} = \sum_{i=0}^{63} d_i x_i^2 \tag{7}$$

It should be noted that these estimations do not correspond to the distortion functions HD_{even} and HD_{odd} in (2). However, these estimations provide enough information to update the programmable parameters correctly. The functionality of these estimations can be explained as follows. Suppose that the residual signal d_i contains an odd-order distortion component $C_a x_i^a$ (with a an odd number and C_a a constant). In (6) this term is multiplied by x_i^3, yielding $C_a x_i^{(a+3)}$, where $(a+3)$ is even. Therefore, the summation adds up to a non-zero value and contributes to $\hat{odd}$. On the other hand, the same component $C_a x_i^a$ in (7) will be multiplied by x_i^2, yielding an odd-order term $C_a x_i^{(a+2)}$, which will add up to zero and therefore does not contribute to $\hat{even}$. In a similar way, even order distortion components in d_i will contribute to $\hat{even}$ only.

The final step of the optimization algorithm is to translate the extracted error estimations to updates of the parameters controlling the variable current sources. To reduce the complexity of this multidimensional problem (there are both four input signals ($\hat{o_e}$, $\hat{g_e}$, $\hat{even}$ and $\hat{odd}$) and four output signals (p_1 up to p_4)), available knowledge of the circuit is exploited. First of all, it is known that the T&H circuit is composed of two differential pairs (fig. 1): one main pair (controlled by p_1 and p_2), which is responsible for the basic functionality of the buffer, and a much smaller cross coupled pair (controlled by p_3 and p_4), which has the task to compensate the distortion of the main pair [8]. Consistent with this difference in functionality, the offset and gain errors ($\hat{o_e}$ and $\hat{g_e}$) are used only to update parameters p_1 and p_2, while the distortion estimations ($\hat{even}$ and $\hat{odd}$) are used only to update

p_3 and p_4. In other words, the basic errors of gain and offset control the main differential pair and the non-linearity errors control the cross-coupled pair.

Next to knowledge about the functionality of the circuit, knowledge about the relations between the parameters and the errors was taken into account to simplify the algorithm. Based on circuit simulations, it can be concluded that the error estimations ($\hat{o_e}$, $\hat{g_e}$, $\hat{even}$ and $\hat{odd}$) are monotonous functions of the parameters p_1 up to p_4. In practice, as the mismatches are relatively small, these functions can be approximated by linear functions. Furthermore, the optimum solution is the solution where all the error estimations are equal to zero. This means that in all cases, the sign of the error determines in which direction (positive or negative) the parameters should be updated. Under the assumption that the functions are linear, the magnitude of the update is automatically proportional to the error itself. Overall, this leads to the following update algorithm, where $p_x[k+1]$ is the new parameter, $p_x[k]$ the old parameter and $\Delta_x[k]$ the parameter update:

$$p_x[k+1] = p_x[k] + \Delta_x[k] \text{ , with:} \tag{8}$$

$$\begin{cases} \Delta_1[k] &= -c_1 \cdot \hat{g_e}[k] &- c_2 \cdot \hat{o_e}[k] \\ \Delta_2[k] &= -c_1 \cdot \hat{g_e}[k] &+ c_2 \cdot \hat{o_e}[k] \\ \Delta_3[k] &= +c_3 \cdot \hat{odd}[k] &- c_4 \cdot \hat{even}[k] \\ \Delta_4[k] &= +c_3 \cdot \hat{odd}[k] &+ c_4 \cdot \hat{even}[k] \end{cases} \tag{9}$$

One can see that in these equations, the gain and offset errors control p_1 and p_2 while the distortion errors control p_3 and p_4. The proportionality constants c_1 up to c_4 are chosen such that a fast and stable settling of the parameters can be achieved.

IV. Behavioral Model Simulations

In order to be able to run Monte Carlo simulations, a behavioral model of the open-loop amplifier from fig. 1 was developed in Matlab. Most importantly, the four controllable current sources were modelled as (3). The four transistors composing the two differential pairs were modelled by the relation $I_d = \frac{1}{2}\beta(V_{gs} - V_{th})^2$. The required measurement DAC was modelled as a 6-bit binary DAC, including a mismatch of $\sigma = 5\%$ of the unit elements. Mismatch was added to all components of the amplifier, according to specifications of the technology. A Monte Carlo analysis was performed on 100 circuits. Each circuit was optimized by means of the presented self-measurement and correction algorithm, allowing a maximum of 64 iterations of the algorithm. The achieved performance was validated both before and after optimization by applying an ideal input sinusoid and deriving the gain-error, offset and THD from the output data. Figures 10, 11 and 12 show the results before and after optimization. Also, the nominal performance (achieved for a circuit without mismatch after parameter optimization) is included in the figures. Using (1), it can be concluded that before correction, the offset and gain errors limit the performance to 6 or 7-bit accuracy, while after correction, a performance of more than 10-bit is achieved. Even the outliers can be corrected fully by means of the proposed method. The THD figure shows that despite the large range of mismatch, the THD is compensated to at least -66dB.

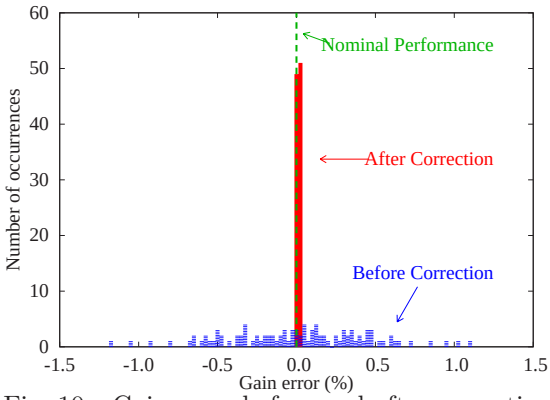

Fig. 10. Gain error before and after correction.

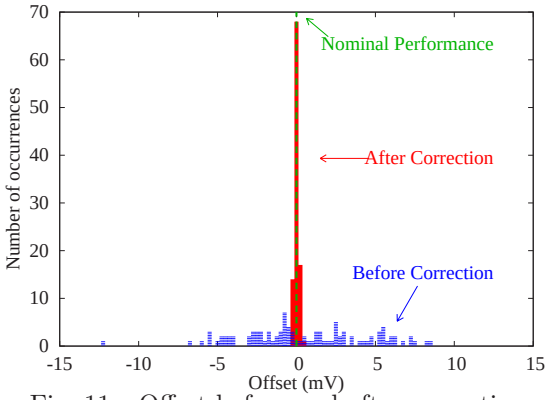

Fig. 11. Offset before and after correction.

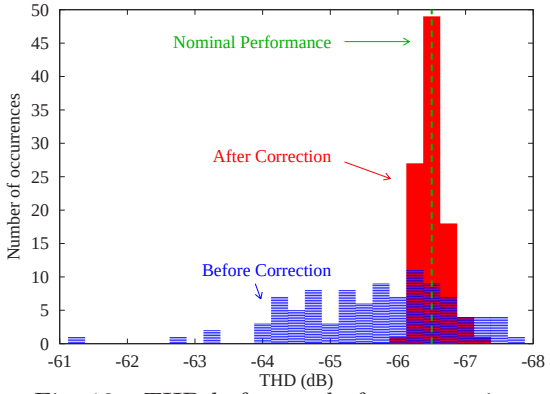

Fig. 12. THD before and after correction.

V. Transistor-Level Simulations

Simulations were performed on a full transistor-level implementation of the T&H circuit as well. Because of computational limitations, only four simulations were carried out. First of all, the optimization algorithm was used on the nominal T&H (without mismatches). Next to that, three simulations were performed with different combinations of mismatch. In each of these cases, mismatch was added to each of the components of the open-loop buffer, being: the four resistors, the four transistors composing the differential pairs and the transistors implementing the four variable current sources. Based on technology information, the σ of each of these components was derived. Extreme mismatch cases were simulated by adding a mismatch of either -3σ or $+3\sigma$ to each component, and choosing only the sign of the mismatch randomly for each component. This approach was repeated three times, resulting in the three mismatch simulations. In all cases, a stable parameter solution was found within 32 iterations of the algorithm. Table I summarizes the results, showing the gain-error, offset and THD both before and after correction. For convenience, the errors are also expressed in equivalent accuracy according to (1). It can be seen that gain and offset errors limit the initial performance to 5 or 6-bit accuracy, but after optimization an accuracy of more than 11-bit is achieved. The final performance is limited by the stepsize of the programmable parameters, and can be further improved by reducing the stepsize. The linearity in terms of THD improves with around 6dB or 1bit, thereby restoring the nominal THD performance. Overall, the T&H becomes suitable for a 10-bit time-interleaved ADC, as the channel mismatches are reduced sufficiently.

TABLE I
Extreme-case transistor-level simulation results.

	gain error		offset		THD	
	%	bit	mV	bit	dB	bit
Nominal	0.00	∞	0.00	∞	-64.0	10.3
Before calibration						
Mismatch 1	1.32	6.2	8.90	5.8	-58.6	9.4
Mismatch 2	1.65	5.9	12.53	5.3	-57.9	9.3
Mismatch 3	0.29	8.4	-16.86	4.9	-54.8	8.8
After calibration						
Mismatch 1	0.04	11.2	-0.09	12.5	-62.4	10.1
Mismatch 2	0.04	11.4	0.07	12.8	-63.8	10.3
Mismatch 3	0.02	12.4	-0.12	12.0	-63.1	10.2

VI. Conclusion

In this paper, a method for the on-chip measurement and correction of gain errors, offsets and nonlinearities of the T&H circuit of an ADC was presented. The method is suitable for on-chip implementation, as it does not require an accurate reference source or an accurate measurement device. The actual correction is performed in the analog domain, such that no additional processing power is consumed at runtime. Extensive simulations confirm a performance improvement of 5bit with respect to gain and offset errors, and a THD improvement of 6dB. As a result, next to high-speed and low-power operation, also high-accuracy and accurate channel-matching can be achieved by the open-loop T&H circuit without increasing the power consumption.

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