A 14mW 500MSPS 59dB SFDR Open-Loop Track-and-Hold Circuit

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***Abstract*— This paper presents the design and implementation of an open-loop Track-and-Hold circuit in a CMOS 0.18μm technology. Also, experimental measurement results are discussed. The open-loop architecture is motivated by the fact that it can potentially reduce the power consumption, increase the speed of operation and improve the portability to new process generations. The limited linearity, related to open-loop structures, is improved by applying a combination of three linearization techniques: source degeneration and cross-coupling of the output buffer and clock-boosting of the sampling switches.**

The simulation and measurement results reveal that the presented T&H achieves a high sampling speed of 500MSPS while consuming 14mW at a 1.8V power supply. Because of the linearization techniques, an SFDR of 59dB is obtained. Moreover, the simplicity of the open-loop structure allows simple migration to future process generations. Benchmarking reveals that the proposed open-loop architecture provides a suitable solution for state-of-the-art AD converters.

I. Introduction

This paper presents the design, implementation and experimental verification of an open-loop T&H circuit. Parts of this work were presented before in [1], [2]. The current state-of-art in T&H design is discussed in section II, and a design goal is specified in section III. The overall T&H architecture is introduced in section IV, while the architectures for the sampling core and output buffer are discussed in section V and section VI, respectively. The final design is presented in section VII and experimental results are discussed in section VIII. Finally, conclusions are drawn in section IX.

II. Literature review

In most cases, T&H circuits are not published as a separate component, but as an integral part of a complete ADC. Because of that, limited information could be found on the performance of the T&H circuits itself. An overview of recent work on T&H circuits was made, considering experimentally verified CMOS implementations only. A summary is included in table I and table II, reviewing closed-loop and open-loop architectures, respectively. For the open-loop solutions, the used topology is indicated by either SF (source follower) or DP (differential pair). Note that the designs of [3] and [4] are realized by time-interleaving 16 channels; the information in the table is for a single channel.

Few publications report the achieved performance in terms of linearity and noise (expressed in SNDR or ENOB); in most cases, only the linearity (expressed in SFDR or THD) is given while noise is neglected. To accommodate for this, two different FoMs are used; one based on the ENOB, and one based on the SFDR:

$$FoM_{ENOB} = \frac{Power}{2^{ENOB} \cdot min(f_s, 2f_{in,max})} , \quad (1)$$

$$\text{with } ENOB = \frac{SNDR - 1.76}{6.02}$$

$$FoM_{SFDR} = \frac{Power}{2^{(SFDR-1.76)/6.02} \cdot min(f_s, 2f_{in,max})} \quad (2)$$

Note that the SFDR-based FoM gives a lower-bound for the ENOB-based FoM, as the SNDR is upper-bounded by the SFDR.

Reference	[5]	[6]	[7]	[8]	[9]
Technology	0.5μm	0.35μm	0.18μm	0.25μm	0.35μm
Power supply	1.2V	3.3V	3.3V	0.5V	3V
Power consumption	1.2mW	320mW	75mW	0.3mW	26.4mW
SFDR/THD	50dB	65dB	78dB	-	66dB
ENOB	-	-	-	9.3bit	-
$min(f_s, 2f_{in,max})$	6MHz	20MHz	90MHz	1MHz	240MHz
FoM-SFDR	774fJ	11pJ	128fJ	-	67fJ
FoM-ENOB	-	-	-	476fJ	-

TABLE I
Overview of recent work on closed-loop T&H circuits in CMOS technology.

Reference	[10]	[11]	[3]	[12]	[4]
Technology	0.35μm	0.35μm	0.12μm	0.18μm	0.13μm
Power supply	3.3V	3.3V	1.2V	1.8V	1.6V
Power consumption	70mW	30mW	2mW	200mW	4.6mW
SFDR/THD	63dB	35dB	50dB	28dB	64dB
ENOB	-	-	7.6bit	-	7.7bit
$min(f_s, 2f_{in,max})$	90MHz	1GHz	100MHz	10GHz	84MHz
FoM-SFDR	674fJ	650fJ	77fJ	975fJ	42fJ
FoM-ENOB	-	-	103fJ	-	260fJ
Topology	DP	SF	SF	SF	SF

TABLE II
Overview of recent work on open-loop T&H circuits in CMOS technology.

When comparing the open-loop and closed-loop solutions with respect to speed, accuracy and FoM, the following can be observed:

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- **Speed**: the open-loop solutions achieve a higher speed (90MHz - 10GHz) compared to the closed-loop solutions ($\leq$240MHz).
- **Accuracy**: on average, the linearity of the closed-loop solutions (50dB - 78dB) is better than the linearity of the open-loop solutions (28dB - 63dB).
- **FoM**: both closed-loop and open-loop solutions can achieve a FoM below 100fJ.

III. Design Goal

Though the T&H is considered as a stand-alone component in this paper, in reality it will be used as the frontend of an ADC. As the ADC targets 8-bit performance at 500MSps, the minimum requirement for the T&H is set to an SFDR of 60dB and a sample rate of 500MSps. Moreover, the requirements for signal-range, common-mode level and expected load are given by the ADC. Aiming at an SFDR-based FoM of 50fJ for the T&H, a first estimation of the power budget of the T&H is set to 25mW. An overview of the design specifications is given in table III. It should be noted that even compared to today's state-of-the-art, the proposed design target is still a challenging goal: the best SFDR-based FoM reported in section II equals 42fJ, which is in the same order as the 50fJ-target. In absolute terms of speed and linearity, the design goal is also at the limit of current solutions as illustrated in fig. 1: only one existing solution achieves a marginally better speed-linearity product.

Supported by the study in the previous section, it was decided to implement the T&H as an open-loop structure. In the next section, the open-loop architecture is introduced.

Technology	0.18μm
Power supply V_{DD}	1.8V
Signal range $V_{in,pp}$	1.0V
Common mode voltage V_{CM}	1.1V
Load	500fF
Power consumption	$\leq$25mW
SFDR	$\geq$60dB
$f_s, 2f_{in,max}$	500MHz
FoM-SFDR	$\leq$50fJ

TABLE III

Design goal of this work.

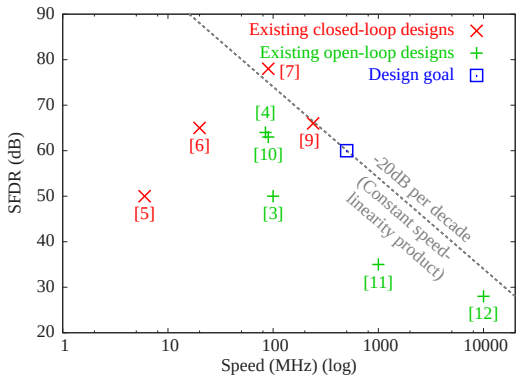

Fig. 1. Speed and linearity of existing T&H circuits and the chosen design target.

IV. T&H Architecture

A general view of a differential open-loop T&H circuit is given in fig. 2. The analog time-continuous input signal is sampled onto the sampling capacitors by means of switches. The switches are controlled by an externally applied clock signal through a switch driver. An open-loop output buffer is used to drive the load (the ADC) without affecting the sampled value at the capacitors.

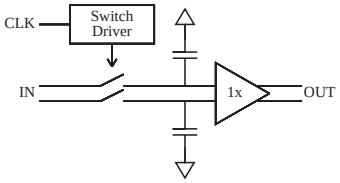

Fig. 2. Open-loop Track&Hold architecture.

It should be noted that this architecture is actually composed of two open-loop structures: the first one is the sampling structure itself (switches, switch drivers and capacitors), and the second one is the output buffer which is to be implemented as an open-loop circuit as well. First, the sampling structure will be discussed in section V. Then, the open-loop buffer will be introduced in section VI.

V. Sampling Core Architecture

The actual core of the T&H circuit is the sampling circuit, composed of the sampling capacitors, switches and switch drivers (fig. 2). The size of the sampling capacitors was set to 200fF, such that for a full-scale input sine ($1V_{pp}$) an SNR of around 64dB is achieved. The switches use the bootstrapping technique presented by [13] to achieve both high speed and high linearity. Using this technique, the actual switch can be implemented with a single NMOS device. High speed is obtained by driving the switch with a high overdrive voltage $V_{gs} = V_{DD} = 1.8$V because of which a small transistor ($\frac{W}{L} = \frac{5\mu\text{m}}{0.18\mu\text{m}}$) can be used as switch, which in turn reduces the parasitic capacitance. As a result of the high overdrive voltage, a small on-resistance is still achieved. Next to that, as the bootstrapping technique generates a constant V_{gs} voltage, independent on the input signal V_s at the switches' source, high linearity is achieved as well. The implementation of the switch driver is shown in fig. 3, which is identical to the design described by [13]: the capacitors are pre-charged to act as an internal 1.8V battery. When CLK is low, the gate of the sampling switch is connected to ground to open the switch. When CLK is high, the 1.8V battery will be connected between the source and the gate of the sampling switch, such that $V_{gs} = V_{DD} = 1.8$V and the switch will be turned on.

Transistor-level simulations were performed on the sampling core (excluding the output buffer), with the implemented capacitors, switches and switch drivers. While a slow input ramp signal was applied to the input, the sampling core was sampling at a rate of 500MSps. The sampled data points were stored for processing. After subtraction of the best-fit line,

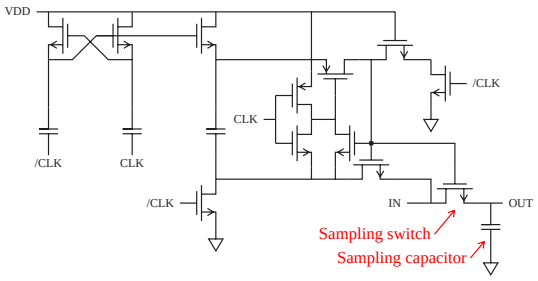

Fig. 3. Bootstrapping technique applied to the sampling switch.

the distortion introduced by the sampling core remains. This distortion curve is plotted in fig. 4. The maximum deviation is only $V_{err,max} = 32\mu$V. This performance can be expressed in terms of effective-number-of-bits (ENOB) by equating this error with 0.5LSB of the full-scale range ($\pm V_{fs}$):

$$ENOB = \log_2 \frac{V_{fs}}{V_{err,max}} , \qquad (3)$$

resulting in an equivalent accuracy of $ENOB = 13.9$bit, which is sufficient for the design goal of about 10bit linearity. The simulated power consumption equals 0.25mW, which is negligible compared to the overall T&H consumption. The performance of the switch-driver was not further optimized as the achieved linearity and power consumption are abundantly better than the expected overall performance.

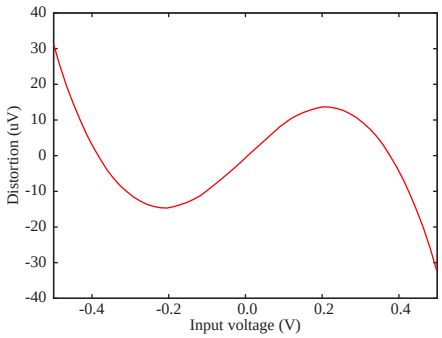

Fig. 4. Simulated distortion of the sampling core, operating at 500MSps.

VI. Output Buffer Architecture

The open-loop output buffer (fig. 5) was implemented with a cross-coupled differential pair with source degeneration, as presented previously in [1]. The basic core is composed of a differential pair with resistive load. In order to improve the linearity, two linearization techniques (known from a.o. [14]) are applied: source degeneration and cross coupling. The first step is to add a source-degeneration resistor to the differential pair. As a second modification, cross-coupling has been applied: a first differential pair (composed of transistors M_1, M_2, M_3, M_4 and source degeneration resistor R_{s1}) is connected as usual. A second differential pair (composed of transistors M_5, M_6, M_7, M_8 and source degeneration resistor R_{s2}) is cross-coupled to the first pair, in other words: the input is in parallel to the input of the first pair, but the output is reversed compared to the first pair. As explained in [1], the two differential pairs can be designed such that the distortion of the first pair is partially compensated by the distortion of the second pair, thereby realizing a higher linearity for the overall transfer characteristic.

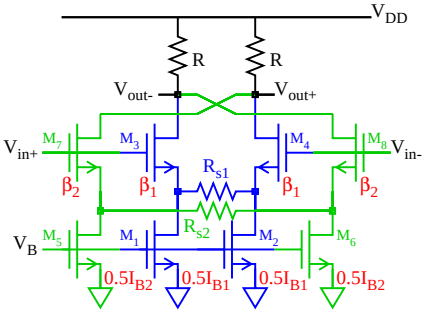

Fig. 5. Cross-coupled differential pair with resistive source degeneration.

The parameters in the final design are summarized in table IV, while the simulated performance is visualized in fig. 6. This figure shows the DC transfer function of the differential pair after subtraction of the linear term, such that only the distortion components remain. Also, a polynomial approximation is shown, which is composed of a third-order and a fifth-order term. As the polynomial approximation matches the simulated curve closely, it can be concluded that the third-order and fifth-order distortion are still dominating the overall linearity. The simulation results reveal that the maximum deviation was reduced to $V_{err,max} = 0.57$mV, resulting in $ENOB = 9.8$bit, which suits the 60dB SFDR-goal. More precise linearity simulations will be presented later in this work, when the sampling core and output buffer will be simulated together.

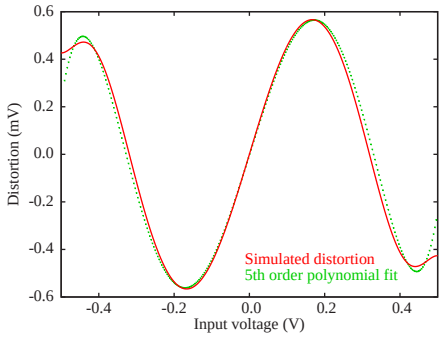

Fig. 6. Simulated distortion of the output buffer.

VII. Simulation Results

This section presents the simulation results of the open-loop T&H circuit, composed of the sampling core and the open-loop output buffer, as introduced in the previous two sections. Transistor-level simulations were carried out in the time-domain to analyze the properties of the presented circuits. A 500MHz sampling clock was applied to the T&H, while sinusoids of various frequencies were applied as an input signal.

TABLE IV

PARAMETERS OF THE OUTPUT BUFFER.

Parameter	Value
I_{B1}	7.8mA
I_{B2}	0.3mA
R_{s1}	307Ω
R_{s2}	1.7kΩ
W/L M_1,M_2	45.0μm/0.18μm
W/L M_3,M_4	39.6μm/0.18μm
W/L M_5,M_6	1.2μm/0.18μm
W/L M_7,M_8	13.2μm/0.18μm
R	167.5Ω

The static linearity (fig. 7) is limited by the output buffer (62dB), as the linearity of the sampling structure (86dB) is far better. The dynamic linearity was determined by means of the achieved SFDR (Spurious-Free-Dynamic-Range) as a function of f_{in} (fig. 8). It can be observed that the target SFDR of 60dB is achieved for the whole Nyquist band.

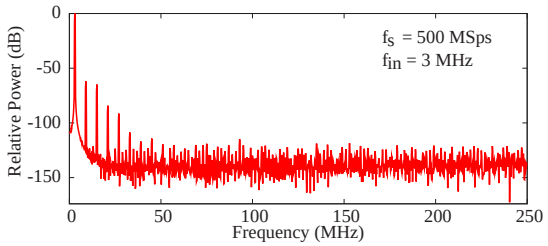

Fig. 7. Output spectrum of the T&H.

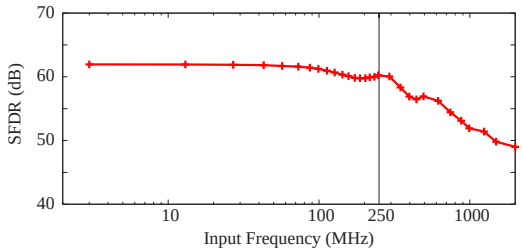

Fig. 8. SFDR (linearity) as a function of the input frequency.

Table V summarizes the simulated features of the T&H. Fig. 9 shows the layout of the implemented T&H, measuring 90μm x 90μm.

TABLE V

FEATURES OF THE OPEN-LOOP T&H CIRCUIT.

	Differential Pair
Sampling speed	500MSps
Static accuracy	62dB
Dynamic accuracy (1GHz)	52dB
Power consumption	14.4mW

VIII. EXPERIMENTAL RESULTS

A. Measurement setup

To evaluate the performance of the T&H circuit at full-speed without an integrated ADC, on-chip subsampling was

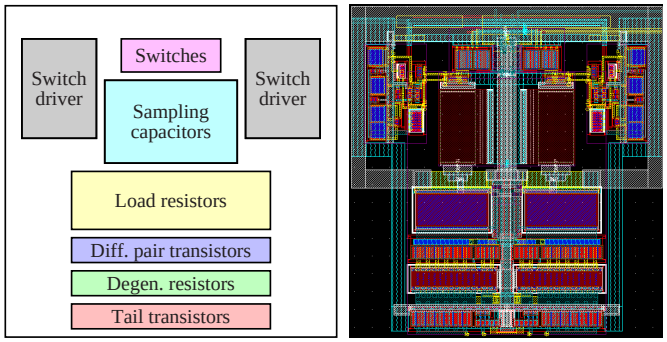

Fig. 9. Floorplan and layout of the T&H. The shown area is 90μm x 90μm.

applied (fig. 10): a first T&H operates at the intended speed of 500MSps. Then, a second (identical) T&H in the same chip is connected to the output of the first T&H. The second T&H samples the output of the first T&H. However, the second T&H operates at a lower sampling rate by resolving only one out of many samples of the first T&H. During the experiments, a subsampling factor of 3328 was used, yielding a sample rate of 150kSps for the second T&H while the first T&H operates at 499.2MSps. The subsampling factor is chosen such that the first T&H operates at the intended speed, while the speed of the second one is reduced to such an extent that it can safely drive the off-chip parasitics and an external off-the-shelf ADC. An important drawback of the subsampling setup is that the measured performance at the output contains the imperfections of two T&H's and an ADC. Therefore, the experimental results will yield a lower bound for the actual performance of a single T&H.

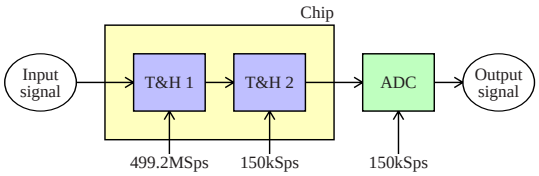

Fig. 10. Subsampling method to facilitate off-chip AD conversion.

A custom setup was put together for the T&H measurements, a photo of the PCB that is used to interface to the test-chip is shown in fig. 11.

B. Measurement results

For the evaluation of the dynamic performance of the T&H, full-scale input sinusoids of various frequencies were applied to the T&H. Based on the measurements, the SFDR and the ENOB (using the SNDR) were derived. The results are shown in figures 12 and 13, respectively. The SFDR (fig. 12) remains above 59dB throughout the Nyquist range. As visualized in the figure, the SFDR is limited by either 2^{nd}, 3^{rd} or 5^{th} order distortion, dependent on the input frequency. This dependency is not in agreement with the simulation results, where the linearity was invariably limited by the 3^{rd} order

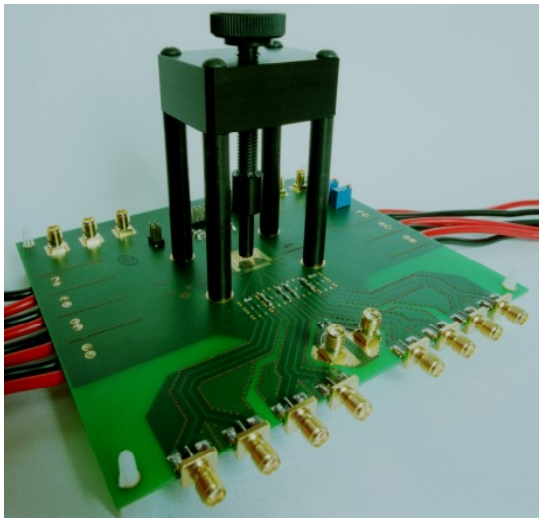

Fig. 11. PCB for the T&H measurements.

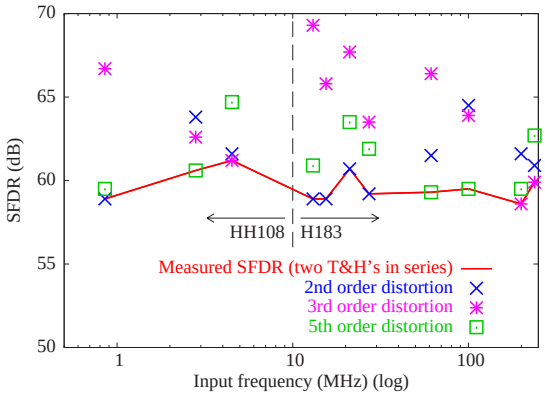

Fig. 12. Measured SFDR of the T&H circuit, operating at 500MSps.

distortion component. The most likely cause of this effect is related to the network driving the input of the T&H, which is composed of the signal generator, low-pass filter, transformer, cables, PCB traces and termination network. In the presented implementation, the sampling switches of the T&H (see fig. 2) are connected directly to the bondpads and the external network. At the sampling instant, the charge in the channel of the switch-transitor has to be drained; a part of this charge will flow into the sampling capacitor and a part will flow into the input network, which includes the external circuitry. The distribution of the charge depends on the impedances seen on both sides of the switch. Whenever the external impedance changes, it will affect the charge distribution which in turn can affect the linearity. Due to the limited bandwidth of the external components, its impedance will vary as a function of the applied frequency, which explains the obtained frequency-dependent SFDR. Most notably, two different transformers were used to convert the single-ended input signal to a differential one: a *Macom HH108* with a bandwidth of 200kHz-30MHz was used for the lower signal frequencies, and a *Macom H183* with a bandwidth of 30MHz-3GHz was used for the higher signal frequencies, as indicated in fig. 12. From the measurements it appears that at the lower-end of the bandwidth of the transformers (0.85MHz for the HH108 transformer and 13 - 27MHz for the H183), the dominant distortion is of 2^{nd} order. This corresponds to the fact that for the lower-end of the bandwidth, the transformers exhibit an increased mismatch between the differential outputs, causing asymmetry in the input signal applied to the T&H. Because of that, even-order distortion dominates over odd-order distortion for these frequencies. In conclusion, it is most likely that the linearity is limited by the effect of the input network on the sampling structure and not by the differential-pair output buffer. Nonetheless, a 59dB SFDR could be maintained, which is close to the intended 60dB SFDR.

As shown in fig. 13, the measured ENOB can be approximated by a simple first-order model that assumes 8.4bit static accuracy and 3.8ps clock jitter. This model can be expressed as:

$$ENOB = \frac{10\log_{10}\frac{1}{\frac{1}{SNDR_{static}}+\frac{1}{SNDR_{jitter}}} - 1.76}{6.02}, \quad (4)$$

where $SNDR_{static}$ models the static performance and $SNDR_{jitter}$ models the jitter performance. These terms can be expressed as a function of the static accuracy in bits (N_{static}), the time-skew (σ_t), and the input frequency (f_{in}):

$$\begin{cases} SNDR_{static} &= 10^{(6.02N_{static}+1.76)/10} \\ SNDR_{jitter} &= \left(\frac{1}{2\pi f_{in}\sigma_t}\right)^2 \end{cases} \quad (5)$$

To obtain the proposed model in fig. 13, the parameters are set to $N_{static} = 8.4$bit and $\sigma_t = 3.8$ps. In the following, it will be explained why the experiments yield these figures.

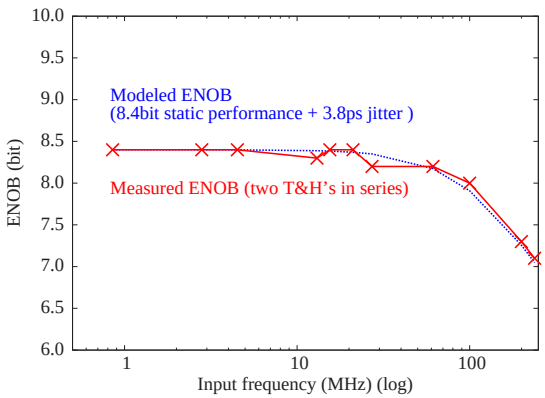

Fig. 13. Measured ENOB of the T&H circuit, operating at 500MSps.

First, the jitter performance will be investigated. The most likely cause of jitter is noise generated in the switch driver. Therefore, a transient noise analysis using the Mentor Eldo simulator was performed on the sampling core. Calculating the time average of the RMS noise for a 0.5V, 247MHz input sinusoid results in an average noise-level of 2.2mV$_{\text{rms}}$. As the input signal has a peak amplitude of 0.5V, the achieved SNR at this frequency equals 44.1dB. According to (5), this corresponds to $\sigma_t = 4$ps, which is similar to the value of $\sigma_t =$

3.8ps that was derived from the experimental results. Apart from jitter generated inside the chip, it is also possible that the measurement is limited by jitter coming from the signal generator or the clock generator. As the jitter specification of the clock generator is given to be 2ps typical or 5ps maximum, this could also limit the measured result.

As a next step, the achieved static performance will be discussed. From the experiments, an ENOB of 8.4bit could be observed, which corresponds to an SNDR of 52.3dB. The SNDR considers both noise and distortion power. When splitting these terms from the measured data, the THD and SNR can be derived, yielding a THD of -56dB and an SNR of 55dB. The THD value is to be expected, as the measured SFDR (considering only the dominant distortion component) equals 59dB. When adding all distortion components together, the resulting THD should be worse than, but relatively close to -59dB. For the SNR, there are two contributions to be considered: the first one is kT/C noise from the sampling structure, the second one is the noise of the buffer stage. From section V and section VI, it is known that both contributions are equal to 64dB, resulting in a combined SNR of 61dB. On top of that, two T&H circuits are used in series during the experiments, so the total input-referred SNR is expected to be 58dB, which is reasonably close to the measured result of 55dB.

A summary of the measured performance is included in table VI. For comparison with prior art, the FoM-SFDR and FoM-ENOB are also calculated. As the T&H is designed for Nyquist operation, the ERBW should be equal to 250MHz. At this frequency, the measured ENOB equals 7.1bit. As a 0.5bit performance-loss is typically allowed at the ERBW, an ENOB of 7.6bit can be claimed in combination with a 250MHz ERBW. For the calculation of the FoM-ENOB, the latter ENOB is used as well. When comparing the measured result with the original design goal (table III), it appears that all requirements could be fulfilled except for the linearity which is 1dB less compared to the target. However, the SFDR-based FoM of 37fJ is still better than expected as the achieved power consumption of 13.5mW is substantially better than the goal of 25mW. Also, as explained previously, the most likely cause of the limited linearity is because of the measurement setup, and not because of the T&H itself.

Power supply V_{DD}	1.8V
Signal range $V_{in,pp}$	1.0V
Power consumption	13.5mW
$f_s, 2f_{in,max}$	500MHz
SFDR (DC - Nyquist)	59dB
Low-frequency ENOB	8.4bit
ENOB at Nyquist	7.1bit
ENOB for ERBW equal to Nyquist	7.6bit
FoM-SFDR	37fJ
FoM-ENOB	139fJ

TABLE VI

MEASURED PERFORMANCE OF THE T&H.

IX. CONCLUSION

In this paper, an open-loop Track-and-Hold circuit designed in a CMOS 0.18μm technology was presented. Because of the open-loop architecture, a high speed of 500MSps could be achieved. At the same time, by introducing a cross-coupled source degenerated differential pair, a high-linearity of 59dB SFDR could be realized.

The experimentally verified performance in terms of the FoM-ENOB, the FoM-SFDR or the speed-linearity product is comparable to the current state-of-the-art. The main performance limitation of the current implementation is due to jitter noise of the switch driver. This limits the ENOB at Nyquist to 7.1bit, which is a loss of 1.3bit compared to the static ENOB. By increasing the power consumption of the driver, the jitter noise could be reduced in order to improve the ENOB at Nyquist. As the power consumption of the driver (0.25mW) is small compared to the overall consumption (13.5mW), reducing the jitter would have little impact on the power budget. Therefore, it is expected that a further improvement of the FoM-ENOB is possible.

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